EE/CprE/SE 491 WEEKLY REPORT

Feb 3rd – Feb 18th

Group number: Sdmay23/44

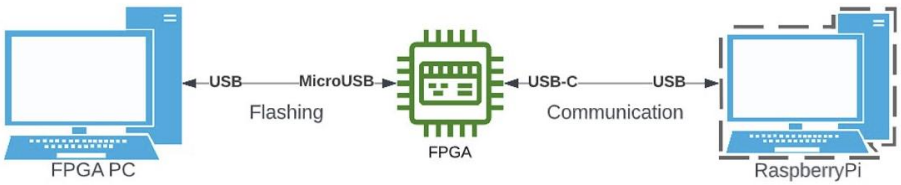
Project title: Mr. Ohm

Client &/Advisor:

- Client: Daniel Walker
- Advisor: Nathan Neihart

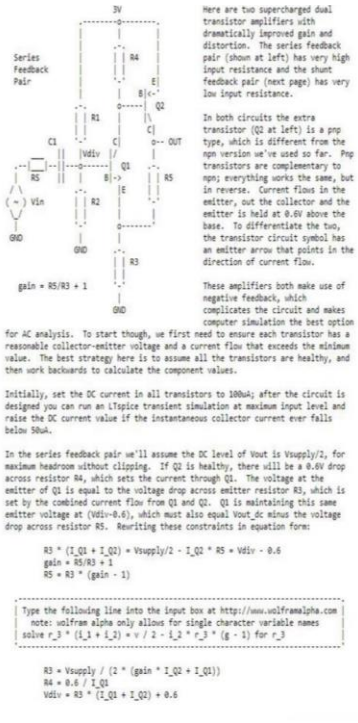
Team Members/Role:

1. Weekly Summary
    - Our team has made progress in setting up the development environment, USB recognition, amplifier circuit improvements, and obtaining a resource to order fabricated boards. However, they still have pending issues such as opening UART shell over our FPGA's internal USB bridge, working on the camera subsystem, finalizing the ADC design, and redesigning the amplifier circuit. The team members have individual contributions and plans for the upcoming week, such as working on PCB design, getting the processor to host a UART shell, and creating a PCB layout for the updated amplifier circuit. The weekly advisor meeting was productive, with Nathan Neihart guiding and reminding the team of important considerations for the PCB design phase, leading to a realignment of the team and a confident plan for the project's future.
2. Past Week Accomplishments
    - Raj Singh:
        - Setup development environment for communication between the Raspberry Pi and FPGA



        - Facilitated meetings and discussions.
        - Able to adjust LED settings using USB Firmware
        - Able to read PMOD Information using USB-C Firmware
    - Jordan McGhee:
        - USB device was recognized by a Linux platform
        - Successfully uploaded and ran custom firmware to the processor
        - Altered orbtrace code to work with our FPGA platform
    - Tyler Smith:
        - Successfully built amplifier circuit to match closely with ideal amplifier. This was before any stability issues were brought up with getting the poles and zeros to match up from the input and output.
    - Rachel San Agustin:
        - Familiarization with EasyEDA – schematic/PCB editor to be used for prototyping, preferred by the client.

- Clarified footprint & component specifications with client
- Obtained resource through which to order fabricated board (JLC)



Here are two supercharged dual transistor amplifiers with dramatically improved gain and distortion. The series feedback pair (shown at left) has very high input resistance and the shunt feedback pair (next page) has very low input resistance.

In both circuits the extra transistor (Q2 at left) is a pnp type, which is different from the npn version we've used so far. Pnp transistors are complementary to npn; everything works the same, but in reverse. Current flows in the emitter, out the collector and the emitter is held at 0.6V above the base. To differentiate the two, the transistor circuit symbol has an emitter arrow that points in the direction of current flow.

These amplifiers both make use of negative feedback, which complicates the circuit and makes computer simulation the best option for AC analysis. To start though, we first need to ensure each transistor has a reasonable collector-emitter voltage and a current flow that exceeds the minimum value. The best strategy here is to assume all the transistors are healthy, and then work backwards to calculate the component values.

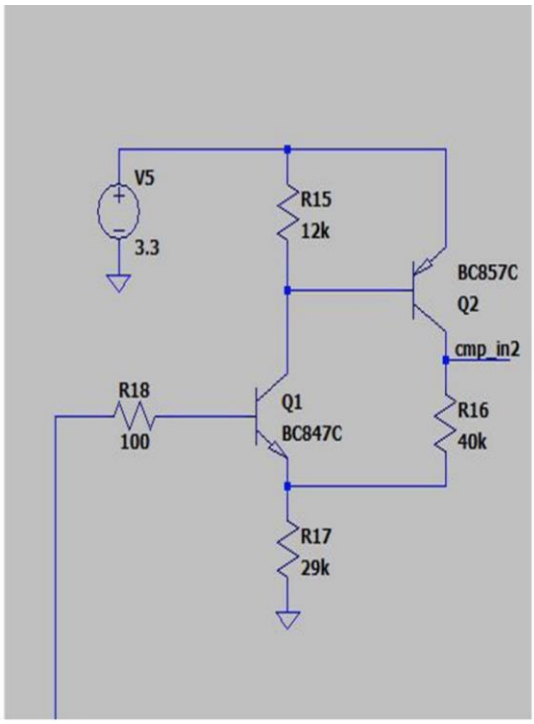
Initially, set the DC current in all transistors to 100uA; after the circuit is designed you can run an LTspice transient simulation at maximum input level and raise the DC current value if the instantaneous collector current ever falls below 50uA.

In the series feedback pair we'll assume the DC level of Vout is Vsupply/2, for maximum headroom without clipping. If Q2 is healthy, there will be a 0.6V drop across resistor R4, which sets the current through Q1. The voltage at the emitter of Q1 is equal to the voltage drop across emitter resistor R3, which is set by the combined current flow from Q1 and Q2. Q1 is maintaining this same emitter voltage at (Vdiv-0.6), which must also equal Vout_dc minus the voltage drop across resistor R5. Rewriting these constraints in equation form:

```
R3 * (I_Q1 + I_Q2) + Vsupply/2 - I_Q2 * R5 + Vdiv - 0.6
gain = R5/R3 + 1
R5 = R3 * (gain - 1)
```

```
Type the following line into the input box at http://www.wolframalpha.com
  note: wolfram alpha only allows for single character variable names
solve r_3 * (i_1 + i_2) + v / 2 - i_2 * r_3 * (g - 1) for r_3
```

```
R3 = Vsupply / (2 * (gain * I_Q2 + I_Q1))
R4 = 0.6 / I_Q1
Vdiv = R3 * (I_Q1 + I_Q2) + 0.6
```



3. Pending issues
    - Figure out how to open UART shell over internal USB bridge
    - Start developing camera subsystem in Lite-X
    - Finalize ADC design
    - Need to redesign amplifier circuit using the bias current from one of the transistors as a dependent variable that can be tweaked to get the same results from last week. Keeping in mind the location of the poles and zeros to ensure stability within the circuit.
    - For the amplifier, what parameters should be used in the FPGA. (1. Voltage Range: 0 to Vmax, 2. Threshold Voltage: shifts the input to zero so that anything above and below deems logic “high” and “low”.)

4. Individual Contributions

Name	Individual Contributions	Hours this week	Hours cumulative
Raj Singh	Facilitating, FPGA	4	80
Jordan McGhee	FPGA	6	100
Rachen San Agustin	ADC	2	50
Tyler Smith	ADC	3	67

5. Plans for the upcoming week
    - Raj Singh:

        - Work on developing test code for transmitting data between the FPGA and Raspberry Pi
        - Work on PCB design of ADC
    - Jordan McGhee:
        - Work on getting the processor to host a uart shell over one of the usb endpoints
        - Improve developed firmware to allow reading/writing to arbitrary registers
    - Tyler Smith:
        - Get the amplifier to work as previously done. Making sure to keep in mind the clients concerns and feedback. Keeping FPGA teammates updated about the results of circuit based off datasheet recommendations.
    - Rachel San Agustin:
        - Create PCB layout from updated amplifier circuit.
        - Construct breadboard prototype for amplifier circuit
6. Summary of weekly advisor meeting
    - Every Tuesday, our advisor Nathan Neihart meets with our team to discuss our project progress and any issues we may be facing. During our most recent meeting, we delved into some challenges we were experiencing with our ADC design. However, this turned out to be a great opportunity for us to realign and reorient ourselves as a team, as Nathan reminded us of the important considerations, we need to consider during the PCB design phase. Thanks to Nathan's guidance and support, we got back into sync and confidently planned for our project's future.