EE/CprE/SE 491 WEEKLY REPORT

Mar 5th – Mar 23th

Group number: Sdmay23/44

Project title: Mr. Ohm

Client &/Advisor:

- Client: Daniel Walker
- Advisor: Nathan Neihart

Team Members/Role:

1. Weekly Summary
    - Our team made significant progress in various areas of the project last week, including the amplifier circuit, USB communication, and PCB design. This week, we've been focused heavily on the PCB design of the ADC, which is vital for establishing physical connections between the ADC and FPGA, as well as analog signals. As we're nearing our deadline, it's crucial to finalize the ADC design for testing and fabrication. While we were able to design the intended circuit in KiCad to prepare for physical development with a PCB, we discovered issues with the amplification circuit and received feedback from our advisor, which required significant revisions before we could proceed. On the FPGA side, we successfully communicated over USB to the FPGA using a standard Python USB library, as well as through a processor lead UART shell. It was noted in the meeting with the client that both systems could be used and we should opt for the faster of the two.

2. Past Week Accomplishments
    - Raj Singh:
        - Planning out the connection points of the PCB, you're ensuring that the physical connections between the ADC and FPGA are properly established. The bill of material was created for the circuit, while the layout ensures that the components are placed correctly on the PCB. Designing aspects of fabrication in KiCad helps you identify potential issues early on and plan for the physical development of the PCB.
    - Jordan McGhee:
        - Worked on debugging communication between the raspberry pi and the FPGA. Was able to get proper communication through direct USB DMA, and from a UART shell running between the RISC-V core and raspberry pi. Slightly modified FPGA bitstream in order to fix both issues.
    - Tyler Smith:
        - Worked with client to bias amplifier circuit in terms of values like current collector and VBE to come up with resistor values. This will allow each transistor in the circuit to operate in its linear region of operation or also know as the forward active region. This where we want our transistors to be in order for amplification purposes.

3. Pending issues
    - Need to redesign passive circuit due to new amplifier results. Pole frequencies are not the same as I calculated from two weeks ago. Possible hiccup in calculations. Need to confirm with client if this was a math hiccup or something else. Because the second pole frequency is supposed to be 5x greater than the first for stability purposes.

4. Individual Contributions

| Name | Individual Contributions | Hours this week | Hours cumulative |
|---|---|---|---|
| Raj Singh | Facilitating, FPGA | 5 | 87 |
| Jordan McGhee | FPGA | 5 | 108 |
| Tyler Smith | ADC | 5 | 75 |

5. Plans for the upcoming week
    - Raj Singh:
        - To ensure the successful development of our project, it's critical to finalize the parts and schematic for the ADC in KiCad accurately. This process involves carefully selecting the right components to include in the circuit and placing them correctly on the PCB. With the right components in place, it's also necessary to create a well-organized schematic that accurately represents the ADC's functionality and connections. By finalizing the parts and schematic in KiCad, we can ensure that our project will meet our performance and functionality goals while also being easy to manufacture and test.
    - Jordan McGhee:
        - Measure the speed of bulk transfers between the two available methods of communication (Processor UART, USB DMA).
        - Get an outline ready for standard running procedure communicating to and from the board. (Preparation for when the ADC is connected)
        - Integrate FPGA portion of ADC into design per client recommendation https://www.latticesemi.com/products/designsoftwareandip/intellectualproperty/referencedesigns/referencedesign03/simplesigmadeltaadc
        - If time allows begin working on Digital block to simulate camera input.
    - Tyler Smith:
        - Redesign Passive circuit with new/correct pole frequencies and zero frequency. Breadboard passive circuit to confirm LTSPICE results (Transient Analysis). Bias amplifier circuit correctly. Breadboard active (amplifer) circuit running transient and ac analysis. This includes getting the passive components from the ETG. Helping out with PCB where I am able to.
6. Summary of weekly advisor meeting

This week, we had a weekly meeting with our advisor, Nathan Neihart, where we discussed the challenges we encountered in finalizing the fabrication of our ADC design. The incorporation of potentiometers into the design led to some issues in the PCB design, which was an unconventional approach. Despite these difficulties, Nathan provided us with valuable guidance and support, which

helped us refocus as a team and prioritize critical aspects of the PCB design phase. Although the meeting presented some challenges, we came out of it with a more definite plan and a renewed sense of confidence in the project's prospects.