EE/CprE/SE 491 WEEKLY REPORT

Mar 23rd– Apr 7th

Group number: Sdmay23/44

Project title: Mr. Ohm

Client &/Advisor:

- Client: Daniel Walker
- Advisor: Nathan Neihart

Team Members/Role:

1. Weekly Summary
    - Last week was a productive one for our team, with progress made in the areas of, the amplifier circuit, USB communication, and PCB design. This week, we have been focusing heavily on the PCB design for the ADC, which is crucial for establishing physical connections between the ADC and FPGA. With our deadline approaching, finalizing the ADC design for testing and fabrication is crucial. However, during the design process in KiCad, we encountered issues with the amplifier circuit and received feedback from our advisor that required significant revisions before we could proceed. On the FPGA side, we were able to create a unique digital design block that we will use to simulate the camera sending information to the digital portions of the design. As well as this, we were able to integrate the verilog for the decimator and actual conversion of the analog signals.
2. Past Week Accomplishments
    - Raj Singh:
        - Imporoved ADC, after several iterations and feedback both passive and active ADC schematics were finalized, and the ADC was improved to meet the desired specifications. The process of ordering parts and fabricating the board at the ETG was done with great attention to detail.
    - Jordan McGhee:
        - Created unique digital block for simulating camera system.
        - Altered physical design to integrate digital ADC components onto the FPGA and created a wrapper to right the results to memory.
        - Debugging critical error with LVDS signals not mapping to proper IO blocks on the FPGA.
    - Tyler Smith:
        - Reworked circuit components in simulation-based on clients preferences and recommendations. The passive circuit was reworked to accurately represent poles and zeros. This was with the thought process that since we will be breadboarding this circuit first, parasitic capacitances need to be taken into consideration. Those values can be anywhere in the range of 22-30pF from the oscilloscope and board itself. So, capacitor values were increased to prevent this issue. The active circuit or also known as the amplifier circuit, was biased with the help of the client but also other group members. This was done by doing multiple sweeps on 3 values to

pretty much force the value of gain and bandwidth we were looking for. The data was extracted and put through a python code that helped narrow down which runs gave us the data range/parameters we were looking for.

3. Pending issues
    - Raj Singh:
        - Updating development environment.
    - Jordan Mcghee:
        - LVDS Signal integration within the device.
        - Constructing a bitstream that will allow us to conduct testing
    - Tyler Smith:
        - Still need to breadboard both passive and active circuit. This will help determine if our circuits operate correctly with the right valued components. Still a possibility to push gain and bandwidth to further improve the amplification ability of the circuit.

4. Individual Contributions

Name	Individual Contributions	Hours this week	Hours cumulative
Raj Singh	Facilitating, FPGA	5	92
Jordan McGhee	FPGA	8	116
Tyler Smith	ADC	8	93

5. Plans for the upcoming week
    - Raj Singh:
        - With the board set to arrive in the next couple of days, I will have to solder the parts using solder paste and pass it on to Tyler Smith for testing. This should take a great bit of time considering the small footprint of the PCB's. I expect this to take a lot of time. In addition, I have to setup a testing facility at Coover with our ADC and FPGA. This will allow Jordan to conduct further testing on the FPGA ADC connection.
    - Jordan McGhee:
        - Help set up development environment for physical testing.
        - Alter existing design to map ADC to correct physical pins and display the result.
    - Tyler Smith:
        - Breadboard both circuits and try to push amplifier further to achieve greater results. Addition to possible dampening resistor at the base of each transistor due to switching up our transistors. Start writing documentation of all progress, challenges and other important information of project.
6. Summary of weekly advisor meeting

During our weekly meeting with our advisor, Nathan Neihart, we discussed the obstacles we faced in finalizing the fabrication of our ADC design. The inclusion of potentiometers in the design created some

problems in the PCB design, which was an unconventional approach. Nevertheless, Nathan's guidance and support were invaluable, helping us as a team to refocus and prioritize critical aspects of the PCB design phase. Despite the challenges presented during the meeting, we emerged with a clearer plan and renewed confidence in the project's potential.